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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/589,133	08/11/2006	Adil Koukab	90500-000089/US	5444
30593	7590	01/04/2008	EXAMINER	
HARNESS, DICKEY & PIERCE, P.L.C. P.O. BOX 8910 RESTON, VA 20195				JOHNSON, RYAN
ART UNIT		PAPER NUMBER		
		2817		
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/589,133	KOUKAB ET AL.
	Examiner	Art Unit
	Ryan J. Johnson	2817

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on _____.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 19-36 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 19-36 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 11 August 2006 is/are: a) accepted or b) objected to by the Examiner.
 - Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)
 Paper No(s)/Mail Date 8/11/06.
- 4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application
- 6) Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

2. The abstract of the disclosure is objected to because it is longer than 150 words. Correction is required. See MPEP § 608.01(b).

Claim Objections

3. Claim 22 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 22 recites that the linearization of the frequency versus voltage operating curve is performed during the linear-high gain mode. This, however, is redundant, as Claim 19 recites "using a linearized frequency versus voltage curve ... to a linear high gain mode".

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
5. Claims 19-36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Regarding Claims 19,21,24,25,27,28,29,31 and 32, the language "a plurality of elements tuned by the voltage controlled oscillator" is recited. However, there appears to be no elements actually tuned by the oscillator in the applicant's design. The examiner believes this to mean, "a plurality of elements tuned by a tuning voltage" and is interpreted as such in order to apply art.

7. Regarding Claim 24, the applicant recites "linking said element...". However, there are multiple elements present within the claims. For the purpose of applying art, the Examiner interprets "linking said element" as "linking said additional element".

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 19,20,22 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Allott (U.S. Patent No. 6,747,521) in view of Iadanza et al. (U.S. Publication No. 2004/0263259).

10. Regarding claims 19 and 22, Allot discloses a method for analogue self calibrating of a phase locked loop circuit (Figs.6,9) including a phase frequency detector (133), a charge pump (137,138), a loop filter (144), a voltage controlled oscillator (145), including a plurality of elements (220,224,234; Fig.7) tuned by a tuning voltage (V1), the method comprising comparing an output signal of the phase locked loop with a reference signal frequency entering in the PFD (the PFD compares the output of the

VCO --151, through divider 149 -- with the reference frequency 131), switching a voltage controlled oscillator operating mode, in a first frequency tuning operation enabling to wide locking range, to a linear high gain mode (step 303; col.11,46-49; col.8,34-47), and automatically switching, after locking to an appropriate frequency with the first tuning operation (lock is achieved in step 307; col.57-59), said voltage controlled oscillator operating mode to a zero-gain mode, while keeping the frequency of the voltage controlled oscillator unchanged (in sleep mode, the output voltage V2 is latched, PLL circuitry is shut down, and the oscillator maintains its frequency; col.11,61- col.12,5; col.9,11-29).

11. Allott does not explicitly disclose that the frequency-voltage curve is linear. The Examiner notes that using the linear portion of the frequency-voltage curve of a VCO is well known in the art. Iadanza et al. discloses that utilizing the linear portion of the frequency-voltage curve results in an improved level of control ([0004],[0007]). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the linear portion of the frequency-voltage curve of the VCO of Allott, as disclosed by Iadanza et al., in order to have provided the benefits of improved oscillator control.

12. Regarding claim 20, Allott discloses that after said zero-gain mode, said voltage controlled oscillator operating mode is switched to a low gain mode enabling a fine tuning of the frequency by the phase locked loop for compensating small residual frequency errors (after sleep mode is disengaged --step 315--, the system returns to

normal operation and low gain, integrating mode is enabled --step 307 following steps 301,303 and 305).

13. Regarding claim 26, Allot discloses that the lock time is improved by increasing the current of the charge pump (During coarse tuning, the first charge pump 137 is used, which has a current 10 times the second charge pump; col.8,65-col.9,10)

14. Claims 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Allott (U.S. Patent No. 6,747,521) in view of Iadanza et al. (U.S. Publication No. 2004/0263259) as applied to claim 19 above, and further in view of Justice et al. (U.S. Patent No. 6,496,075). Allot and Iadanza et al. disclose the limitations of claim 19. Allot also discloses isolating the elements from their controlling voltages when the phase locked loop is locked (during sleep while the loop is locked, the memory cell 207 outputs a constant voltage, thus isolating itself from V1) and freezing the elements in a state previously obtained to activate zero-gain mode (memory cell 207 outputs a constant voltage, freezing V2 and the analog memory cell output). Neither Allott or Iadanza et al. discloses breaking the linear frequency-voltage curve into several sections, selecting for each section a corresponding element, or submitting each element to a specific voltage, as required by claim 21, or comparing each element to a reference voltage and depending on the result of the comparison, applying a voltage to each element, as required by claim 23. Justice et al. discloses (Fig.7) using comparators (52) comparing a reference voltage (50) to the tuning voltage output (Vtune). Voltages are output from logic (54) to switches (32) in order to enable capacitors (34). Justice discloses that such

a structure between the loop filter and VCO provides an extension of the linear tuning range with low phase noise (col.6,24-61; Fig.6). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the control circuit, including comparators, reference voltages, logic, and switched capacitors, as disclosed by Justice et al., between the tuning voltage and VCO in the circuit of Allott in order to have provided the benefits of a wide tuning range with low phase noise.

Allowable Subject Matter

15. Claims 24,25 and 27 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

16. Claims 28-36 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

17. The following is a statement of reasons for the indication of allowable subject matter: Regarding claim 24, prior art does not disclose using an additional element, linking the additional element to a fixed voltage, and isolating said additional element. Regarding claim 25, Allott does not disclose circuitry to restart the tuning operations if the loop filter voltage reaches an upper or lower limit. Regarding claim 27, Allott discloses using increased charge pump current during high gain mode, not decreased charge pump current. Regarding claim 28, the offset generators and switch configuration, as claimed, could not be found in prior art.

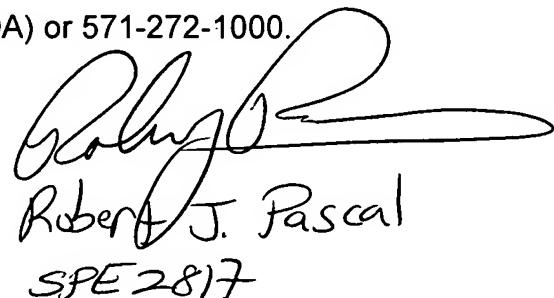
Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yamagishi et al. (U.S. Publication No. 2003/0146794) and Madsen (U.S. Patent No. 5,521,947) disclose PLL's with zero-gain functionality.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan J. Johnson whose telephone number is 571-270-1264. The examiner can normally be reached on Monday - Thursday, 9:00 am - 5:00 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Robert J. Pascal
SPE 2817